Integrated $\mu$-Wireless Communication Platform

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Hardware supporting software to enable applications.
Design Lineage

- COTS dust prototypes (Kris Pister et al.)
- weC Mote (~30 produced)
- Rene Mote (850+ produced)
- Dot (1000 produced)
- Mica node (current, 1800+ produced)
Mote-On-Chip Concept

Develop a single-chip system architecture for wireless embedded devices that:

– Drastically reduces power consumption, cost and size
– Maintains a tight integration between processing, communication, and sensing that allows cross-layer optimizations
– Allows for rich interfaces to hardware accelerators and flexible resource pools
– Provides:
  • Efficiency
    – Through specialized concurrency mechanisms and optimal hardware accelerators
  • Flexibility
    – By using software to compose basic protocol building blocks into application specific protocols with rich interfaces
Integrated Architecture

• Single CPU for Base band, OS and Application
  – Shared system resources can be divided between system components dynamically

• High bandwidth, flexible interfaces can be exposed across system components
  – Allows applications access to fine-grained system control

• Hardware accelerators to support key sensor network challenges
  – Communication, synchronization, power management, concurrency

• Shared memory interface model
First Prototype Layout

- IO Pads
- RAM blocks
- MMU logic
- Debug logic
- ADC
- AVR CPU Core
- RF Place Holder

4 mm² in .25 um CMOS

Core Area only 50% full…
Prototype Tests

AVR Core

Address Translation Unit

Timer Modules

UART

Digital I/O

ADC Controller

RF Serialization

RF Timing

RF Clocking

Channel Monitoring

Address Match Unit

RAM Block

SPI Programming Unit
Power Measurements

Current vs Frequency

- Mica CPU

- Measured
- Trend
- Expected

~ 150 uA/Mhz @ 1.5V
Communication Interface

• Hardware provides ‘AM’ interface
  – Same functionality only implemented in hardware
  – > 5000 x cost reduction
• Hardware handles
  – Message send command with TOSMsgPtr
• Hardware signals
  – Message arrival event with TOSMsgPtr
• CPU communication overhead dropped from approx. 2MIPS down to 0.
• Phil can now run his VM.
Key Comm. Accelerators

- Start symbol detection
- Timing extraction
- DMA memory engine
- Not Included:
  - Channel encoding mechanisms
Memory Management Unit

• Facilitate Network Programming & Multiple Code Images
  – Allocate some frame for OS and some frames for apps.
• CntToLeds < 256 bytes
• Page Frames and Physical Pages Used
  – 32 Page frames w/ 6 physical pages
• Page translation performed automatically
• Highly flexible
• Prevents fragmentation
Integrated ADC

- Ultra low power 8-bit ADC
- 27 pJ per samples
- Designed my Mike Scott

Panasonic is producing 1J battery in 1 mm³

Could take 1000 samples per second for over a year
Second Generation Mote Chip
Second Prototype Block Diagram

- AVR Core
- Address Translation Unit
- RAM Block
- SPI Programming Unit
- Instruction Bus
- Memory Bus
- Reg. windows
- Timer Modules
- UART
- Digital I/O
- ADC Controller
- Encryption
- RF Serialization
- RF Timing
- RF Clocking
- Channel Monitoring
- RF Control Reg.
- RF Freq. Lock
- Address Match Unit
Integrated Transmitter

- 800->1100 MHz transmitter
  - 16 bit frequency steps
- Frequency shift or Amplitude Modulation
- 1Khz frequency accuracy
- Variable frequency separation
- Control registers in I/O space of CPU
- Locked to 32.768 KHz reference crystal
- Inductor and Reference crystal are only external components
Integrated Transmitter (con’t)

• 2.5 V minimum voltage
• 1 mA, .5 mW TX power
  – (compared to RFM .7 mW and 12 mA)
• Targeting 300 uA receive mode (not yet implemented)
• -95 dBm receiver sensitivity
  – Same sensitivity as RFM at 1/10 power
  – Tunable IF (Low)
• <100 us turn-on time
• Designed by Al Molnar
Register Windows

- Allows for fast interrupt support
- With early versions of TinyOS, 50% of CPU energy consumption went to saving register sets
- 32x reduction in interrupt overhead
- 1 User register set, 1 Kernel, Single instruction switch
- Stack preserved across switch
Encryption Support

- Stream based, Bluetooth-like hardware encryption
- Orders of magnitude reduction in encryption cost
- Automatic generation of random pad
- XOR automatically performed during transmission and reception
- Allows for efficient secure communication and authentication
- Encrypted MAC can serve as both CRC check and authentication signature
- Transparent to applications
Current Chip at Fab…
Due back 12/10/2002

- Memory
- 32 KHz Crystal Actuator (1 uW)
- Frequency Control/Lock logic
- 900 MHz trans.
- Core w/ TinyOS support

5 mm² in .25 um CMOS = die cost $.06/mm²
Size Comparison

CC1000
6 mm²

5 mm²

CC1010
Radio + Flash + 8051
19 mm²

Flash